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10/534,164	05/05/2005	Matthias Muth	DE02 0252 US	9960

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EXAMINER	
ZAMAN, FAISAL M	

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
12/10/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/534,164	MUTH, MATTHIAS	
	Examiner	Art Unit	
	Faisal M. Zaman	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-10* is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter "AAPA") and Feuerstraeter et al. ("Feuerstraeter") (U.S. Patent Application Publication No. 2003/0058894).

Regarding Claim 1, AAPA teaches an integrated circuit comprising:

a system base chip configured for communicating over a vehicle data bus using the LIN (Local Interconnect Network) protocol, the system base chip including at least

a system voltage supply,

a system reset, and

a monitoring function (AAPA, page 2, lines 11-14).

AAPA does not expressly teach an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol, and in particular the LIN protocol, that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte, and

a serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit.

In the same field of endeavor (e.g., detection of data transfer rates in a bus system), Feuerstraeter teaches an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte (Feuerstraeter, Figure 4, item 420, paragraphs 0044 and 0047),

A serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit (Feuerstraeter, Figure 3, items 350/360, paragraph 0037).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Feuerstraeter's teachings of detection of data transfer rates in a bus system with the teachings of AAPA, for the purpose of simplifying the ultimate system design; i.e., so that circuit designers could specify one integrated circuit rather than having to combine several circuits.

Regarding Claim 6, AAPA teaches the use of an SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface (AAPA, Page 1, lines 13-17).

The motivation that was used in the combination of Claim 1, super, applies equally as well to Claim 6.

3. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Feuerstraeter as applied to claim 1 above, and further in view of Bongiorno et al. ("Bongiorno") (U.S. Patent No. 6,292,045).

Regarding Claim 2, AAPA and Feuerstraeter teach an oscillator that acts as a clock-signal source and as a timebase for the bit-rate detection (Feuerstraeter, Figure 3, items 480/490, Page 4, paragraph 0044).

AAPA and Feuerstraeter do not expressly teach wherein the oscillator is an R/C oscillator.

In the same field of endeavor (e.g., electrical circuits which use clock sources), Bongiorno teaches the use of an R/C oscillator (Bongiorno, Column 1, lines 16-21).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Bongiorno's teachings of electrical circuits which use clock sources with the teachings of AAPA and Feuerstraeter, for the purpose of providing an RC oscillator which has the ability to generate high frequency oscillations having a stable frequency characteristic.

Regarding Claim 3, Bongiorno teaches wherein the clock signal generated by the R/C oscillator may also be provided to circuits outside the integrated circuit, and in particular to a microprocessor (Bongiorno, Column 1, lines 16-21).

The motivation that was used in the combination of Claim 2, super, applies equally as well to Claim 3.

4. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Feuerstraeter as applied to Claim 1 above, and further in view of Werle (U.S. Patent No. 5,778,002).

Regarding Claims 4 and 5, AAPA and Feuerstraeter do not expressly teach wherein the interface circuit may also pass on complete messages and perform buffer-storage of data received or to be transmitted.

In the same field of endeavor (e.g., multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation), Werle teaches wherein an interface circuit may pass on complete messages by performing buffer-storage of data received or to be transmitted (Werle, Figure 1, item 14, Column 3, lines 13-27).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Werle's teachings of multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation with the teachings of AAPA and Feuerstraeter, for the purpose of reducing latency of the system if the incoming data rate is slower than that which can be processed.

Allowable Subject Matter

5. **Claims 7-10** are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 7, as correctly argued by Applicant (see Response, pages 6-8), the prior art of record does not teach the claimed limitations of "monitor the vehicle

battery voltage; and provide a reset signal in response to the monitoring of the vehicle battery voltage", and also "detect a bit rate for the received analog signals in response to the detected LIN protocol header and with reference to a clock signal; and convert the analog signals to a digital data signal in response to the detected bit rate", in connection with the other limitations in the claim.

Claims 8-10 are allowable due to a dependency on Claim 7.

Prior Art of Record

6. The prior art made of record and not relied upon (cited on the attached PTO-892 form) is considered pertinent to applicant's disclosure.

Response to Arguments

7. Applicant's arguments, see pages 6-8, filed 11/23/2010, with respect to Claims 7-10 have been fully considered and are persuasive. The rejection of 8/23/2010 has been withdrawn.

8. Applicant's arguments filed 11/23/2010 with respect to Claims 1-6 have been fully considered but they are not persuasive.

Regarding Claim 1, Applicant argues that "adding the SERDES chipset of the '894 reference, somehow modified for the LIN-protocol, would result in a solution that is not noticeably different from AAPA, which already provides a multi-chip solution requiring specially adapted chips and microcontrollers and does not correspond to the claim limitations." (Response, page 5, last paragraph). The examiner disagrees.

Contrary to Applicant's argument, it would have in fact been obvious to combine the teachings of Feuerstraeter with AAPA. Although it is believed that the wording that was previously used (i.e., "without using additional hardware") was adequate, the examiner has further clarified the motivation in the rejection above. As discussed in AAPA, the various components were known, however an external microcontroller was needed in order to provide the functionality of the claimed "interface circuit" and "serial/parallel converter". The proposed combination would result in all of the components being disposed in a single "integrated circuit" (as discussed below). As discussed in the Board decision of 1/12/2010 (see page 13), "those of ordinary skill in the electronics art were generally motivated to combine related functions in an integrated circuit for the purpose of simplifying the ultimate system design, i.e., so that circuit designers could specify one integrated circuit rather than having to combine several circuits", and "it would have been obvious to combine the interface and serial/parallel functions of Feuerstraeter with the functions of the AAPA base chip as an 'integrated circuit' to simplify the design and because the combination does not produce any different results." Accordingly, it is clear that one of ordinary skill in the art would have been motivated to combine the teachings of Feuerstraeter with AAPA.

Also regarding Claim 1, Applicant argues that "none of the cited references suggests a LIN-protocol solution with the recited elements arranged in a single integrated circuit." (Response, page 6, second paragraph). The examiner disagrees. Contrary to Applicant's argument, the combination of references does in fact teach the claimed "integrated circuit". As discussed in the Board decision of 1/12/2010 (see

pages 8-9), "Claim 1 does not define the physical structure of the 'integrated circuit.' Claim 1 does not require that the three elements are on the same chip; in fact, the recitation of a base chip indicates that the base chip is a separate chip. Although Figure 1 shows the integrated circuit as a block diagram containing all the elements, claim 1 does not require that the integrated circuit is contained in a package. An 'integrated circuit' can be made of separate integrated circuit elements, a known base chip and a separate interface circuit and a separate serial/parallel converter circuit. Thus, the term 'integrated circuit' in claim 1 does not positively recite that all elements are the same chip or in the same package." Applicant also argues that "the '894 reference appears to teach away from such integration through the use of a frequency configuration unit and a frequency selector unit in each of the chips of the chipset disclosed by the '894 reference". The examiner disagrees. Contrary to Applicant's argument, the serializer 410 and deserializer 405 of Feuerstraeter are clearly combined into a single integrated circuit, see Figure 3, item 340 (i.e., a single unit consisting of both the serializer and deserializer), and paragraph 0042 (i.e., referring to the two components together as a "SERDES device"). Accordingly, it can be seen that the combination of references does in fact teach an "integrated circuit" to the extent that it is claimed.

Therefore, these claims stand as previously rejected.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal M. Zaman whose telephone number is 571-272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm, alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Faisal M Zaman/
Patent Examiner, Art Unit 2111